Appl. No. 10/749,570

Atty. Ref. 88537.0068
Customer No. 26021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Mikko WALTARI
Serial No: 10/749,570
Confirmation No. 8972
Filed: December 31, 2003
For: Variable Clock Rate Analog-to-Digital Converter

Art Unit: 2819
Examiner: Wamsley, Patrick G

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:
Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
January 20, 2006
Date of Deposit
Juanita Soberanis
Name
Juanita Soberanis 1/20/06
Signature Date

DECLARATION UNDER 37 CFR 1.131

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Mikko Waltari, of San Diego, California, declare that:

1. I am the named inventor of the captioned U.S. application.

2. I am informed that U.S. patent 6,909,393 having a filing date of July 30, 2003 was cited in an Office Action in the captioned U.S application, and relied on in rejecting the pending claims of the application.

3. The invention claimed in the captioned U.S. application was described in my Innovation Disclosure Document dated June 3, 2003, a copy of which is attached to this declaration. As such, the invention thereof was complete at least by the date of June 3, 2003, which is a date earlier than the filing date of U.S. patent 6,909,393.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false

statements may jeopardize the validity of the application or any patent issuing thereon.

Respectfully submitted,

Date: 01/20/2006

Mikko Waltari

CONEXANT

Docket No.: 03CXT0015D
Ranking: Approved to File

1. Title of Innovation

Clocking Scheme for an Algorithmic Analog-to-digital Converter

2. Division/platform Information

Digital Infotainment Division

3. Innovator(s)

Name	Innovator Information	
Mikko Waltari	Personal Information : Home Address : 4671 Torrey Circle State : CA Phone : 8583611529 Country of Domicile : US Conexant Contact Information : Address : 9868 Scranton Road, State : CA Phone : 858-713-3612 Email : mikko.waltari@conexant.com Mail Code : SA3-370	City : San Diego Zip : 92130 Fax : Citizenship : US City : San Diego Zip : 92121-1762 Fax : Dept. : 039-327- Supervisor : Mr. Efram Burlingame

4. Problem Solved

This will likely be used in later revisions of Tiger and possibly in the rev A of Mako and Mojo. This innovation is a method to improve the clock rate of an analog-to-digital converter (ADC) that is based on the algorithmic principle. Using this method the sampling rate can be increased 50% or more without losing virtually any accuracy. The method relies on modifying the clock signal going into the ADC and thus minimal or no modifications are needed to the ADC itself.

5. Previous Solutions

Traditionally algorithmic ADCs use clock signals in which every clock pulse has an equal length. Such a signal is typically provided by a crystal oscillator or a PLL.

Prior art publications:

K. Nagaraj, ?Efficient Circuit Configurations for Algorithmic Analog to Digital Converters?, IEEE Tran. CAS-II, pp. 777-785, Dec 1993.

US patent 5,861,832, US patent 5,212,486

6. Solution

An algorithmic ADC uses internal clock signal which is an integer multiple of the ADC sampling rate. It performs the A/D conversion serially starting from the most significant bit (MSB) and proceeding toward the least significant bit (LSB). Between the conversion steps the internal analog residue voltage is amplified by 2^k, where k is the number of bits resolved in one step. Thanks to the amplification the accuracy needed gets relaxed as the conversion proceeds.

The proposed method exploits this fact. It simply makes the clock period longer in the first step giving more settling time for the internal switched capacitor circuitry. The accuracy needed in the next step is smaller and thus the analog signals do not need to settle as well making it possible to shorten the clock period. Using this principle the length of each conversion step can be optimized yielding a shorter total conversion time without scarifying the accuracy.

7. Differences/Advantages Over Previous Solutions

This method uses variable clock period dedicating more settling time to the first operation phases in which the accuracy requirement is the highest. This way the total conversion time can be shortened without degrading the overall accuracy.

The method is related to the one used in pipelined ADCs, in which the circuitry is scaled down in latter pipeline stages to save area and power.

8. Status of Innovation

Under development If "Other", please specify

9. Product or program in which innovation will be used:

Products Used : Decoder, Mako, Tiger, Mojo	Technology Used : A/D
If other, please specify :	**If other, please specify :**

Additional Information :	

10. Has anyone disclosed or does anyone plan to disclose your innovation outside the Company?

○ Yes ● No ○ Don't Know

11. Has anyone proposed or does anyone plan to propose a product or program to a customer which

includes your innovation?

○ Yes ○ No ● Don't Know

12. Innovator signature(s): (Do not use black ink)

_____ **Date :** _____
(MIKKO WALTARI)

Qtr Evaluated: 3Q03
Group: Digital Infotainment Division
Technology:
Sub Technology 1:
Sub Technology 2:
Products:
Innovation Block:

Entered: Anonymous @ 06/03/2003 10:30:19 AM
Modified: Tobi Marshall @ 06/04/2003 02:26 PM